TEXAS INSTRUMENTS

PCI2250 Evaluation Module

User's Guide

2000

PCI Bus Solutions

SCPU005

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Preface

Read This First

About This Manual

This manual is designed to assist the user of the PCI2250 evaluation module (EVM). It provides descriptions of parts, features, and operating requirements of the EVM that are necessary or useful to obtain maximum benefit from EVM use.

How to Use This Manual

This document contains the following chapters:

Chapter 1, *Introduction*, provides a brief description of the EVM, and a bill of materials for the EVM kit.

Chapter 2, *Software Requirements*, details the minimum software requirements for any PC system on which the PCI2250 EVM is to be run.

Chapter 3, *Configuration*, explains secondary bus masters and interrupt routing as related to the edge connectors on the board.

Chapter 4, *Board Configuration*, describes the location and purpose of board components such as pins, jumpers, connectors, and LEDs.

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This book may contain cautions and warnings.

This is an example of a caution statement.

A caution statement describes a situation that could potentially damage your software or equipment.

CAUTION

This is an example of a warning statement.

A warning statement describes a situation that could potentially cause harm to you.

WARNING

The information in a caution or a warning is provided for your protection. Please read each caution and warning carefully.

Related Documentation From Texas Instruments

PCI2250 PCI-to-PCI Bridge Data Manual, TI Literature Number – SCPS051

PCI2250 Implementation Guide, SCPU008

Connecting $\overline{ENUM}$ Terminal to an External Open-Drain Buffer, TI Literature Number – SCPA027

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Contents

Figures

Tables

Chapter 1

Introduction

This chapter provides a brief overview of the PCI2250 evaluation module, along with a bill of materials for the EVM kit.

Topic **Page**

1.1 Introduction

This document is intended to assist the user of the PCI2250 evaluation module (EVM), EVM2250B. Included within this document are instructions detailing the proper setup and configuration necessary to operate the PCI2250 EVM.

1.2 Evaluation Kit Bill of Materials

The PCI2250 EVM consists of the following items:

Item	Nomenclature	Quantity
EVM2250B	PCI to PCI adapter card assembly	1
3.5” Diskette	PCIBus and PCIBus95 utility programs	1

Chapter 2

Software Requirements

This chapter provides the minimum software requirements for any PC system on which the PCI2250 EVM is to be used.

Topic **Page**

2.1 Software Requirements

The EVM2250B evaluation board will work in any system that meets the following requirements:

- ❑ BIOS which supports the *PCI Bridge Specification 1.0*.
- ❑ Operating system that supports the *PCI Bridge Specification 1.0*.

In the majority of today's computer systems, bridge support is built into the BIOS. Many operation systems, like Windows 95/98™ and Windows NT™, have support for bridges.

Chapter 3

Configuration

This chapter explains secondary bus masters and interrupt routing as related to edge connectors on the board.

Topic **Page**

3.1 Configuration

The PCI2250 supports four secondary bus masters. Due to board space, only three masters are supported with the EVM2250B board. The three supported masters can be plugged into three edge connectors labeled P1, P2, and P3. These edge connectors are configured based on the Table 3–1.

Table 3–1. Edge Connector Device ID

Edge Connector	Resistor Installed	Slot ID
P1	R20 R21 (default) R22	0 4 (default) 8
P2	R23 (default) R24 R25	1 (default) 5 9
P3	R26 (default) R27 R28	2 (default) 6 A

The interrupts for each connector on the secondary bus are routed according to the *PCI Local Bus Specification Revision 2.2*, section 2.2.6. Table 3–2 depicts how the interrupts are routed on the EVM2250B evaluation board.

Table 3–2. Edge Connector Interrupt Routing

Edge Connector	Interrupt	Routed on INTX on P1
P1	$\overline{\text{INTA}}$ $\overline{\text{INTB}}$ $\overline{\text{INTC}}$ INTD	$\overline{\text{INTA}}$ $\overline{\text{INTB}}$ $\overline{\text{INTC}}$ INTD
P2	$\overline{\text{INTA}}$ $\overline{\text{INTB}}$ $\overline{\text{INTC}}$ INTD	$\overline{\text{INTB}}$ $\overline{\text{INTC}}$ $\overline{\text{INTD}}$ INTA
P3	$\overline{\text{INTA}}$ $\overline{\text{INTB}}$ $\overline{\text{INTC}}$ INTD	$\overline{\text{INTC}}$ $\overline{\text{INTD}}$ $\overline{\text{INTA}}$ INTB

Chapter 4

Board Configuration

This chapter describes the location and purpose of board components such as pins, jumpers, connectors, and LEDs.

Topic **Page**

4.1 Board Jumpers

Built into the evaluation board is the ability to monitor and test all the capabilities of the PCI2250. There are many jumpers located on the evaluation board (J1 through J12), which allow an engineer to perform tests ranging from measuring power to changing the arbitration of the PCI2250. All of these jumpers are defined in Table 4–1.

Table 4–1. Jumper Definitions

Jumper	Description
J1	P_MFUNC select. This jumper is used to select whether to route P_MFUNC to P_LOCK or P_CLKRUN/HS_ENUM.
J5 & J6	Jumpers J5 and J6 are used to control the mode select inputs to the PCI2250.
J7	S_MFUNC select. This jumper is used to select whether to route S_MFUNC to S_LOCK or S_CLKRUN/HS_SWITCH.
J8	Arbitration support. By cutting the trace across this jumper and installing R10 an external arbiter can be used.
J9	S_VCCP for the PCI2250. This jumper can be used to measure the power consumed through the S_VCCP.
J10	P_VCCP for the PCI2250. This jumper can be used to measure the power consumed through the P_VCCP.
J11	Core VCC for the PCI2250. This jumper can be used to measure the power consumed by the PCI2250 core logic.
J12	S_VIO select. This jumper is used to select between 3.3-V and 5.0-V signaling environments on the secondary bus.

4.2 PCI2250 Mode Select Pins

The PCI2250 has three modes of operation based on the value of the mode select pins MS0 (J6-2) and MS1 (J5-2). Table 4–2 shows the jumper settings for the different modes of operation.

Table 4–2. Mode Select Jumper Settings

J6	J5	P_MFUNC	S_MFUNC	Mode
2–3	2–3	$\overline{\text{HS\_ENUM}}$	$\overline{\text{HS\_SWITCH}}$	TI hot-swap
2–3	1–2	$\overline{\text{P\_CLKRUN}}$	$\overline{\text{S\_CLKRUN}}$	TI clock run
1–2	2–3	$\overline{\text{P\_LOCK}}$	$\overline{\text{S\_LOCK}}$	Intel B2 support
1–2	1–2	$\overline{\text{P\_LOCK}}$	$\overline{\text{S\_LOCK}}$	Intel B3 support

4.2.1 Clock Run Mode

When the PCI2250 is in clock run mode, jumpers J1 and J7 should not be jumpered. The clock run signals can be pulled directly from pin 2 of the jumper headers.

4.2.2 CompactPCI™ Hot Swap

When hot-swap mode is selected, jumpers J1 and J7 should have a jumper between pins 2 and 3, routing the multifunction pins to the CompactPCI test points.

4.2.3 Intel™ Mode

When Intel mode is selected, jumpers J1 and J7 should have a jumper between pins 1 and 2, routing the multifunction pins to the $\overline{\text{LOCK}}$ pins on the connectors.

4.3 LED Indicators

4.3.1 D1 $\overline{\text{ENUM}}$

When the PCI2250 is configured in CompactPCI mode, this LED lights when the $\overline{\text{ENUM}}$ signal is driven low.

4.3.2 D2 HSLED

When the PCI2250 is configured in Compact PCI mode, this LED lights when the HSLED signal is driven low.

4.3.3 D3 C1_PRES

D3 lights when a PCI board that has the $\overline{\text{PRSNT2}}$ pin tied to ground is inserted in connector P1.

4.3.4 D4 C2_PRES

D4 lights when a PCI board that has the $\overline{\text{PRSNT2}}$ pin tied to ground is inserted in connector P2.

4.3.5 D5 C3_PRES

D5 lights when a PCI board that has the $\overline{\text{PRSNT2}}$ pin tied to ground is inserted in connector P3.

4.3.6 D6 EVM3V

D6 lights to indicate that 3.3 V is available on the secondary bus.

4.3.7 D7 PCU3V

D7 lights to indicate that the PCI2250 has power applied to the core logic.

4.4 Power Measurements

In order to measure the current drawn by the core logic or one of the VIO rails of the PCI2250 it is necessary to isolate the power supplied to these pins from the rest of the system. This can be done by cutting the trace that connects the power pins to the system. Jumpers J6, J7, and J8 have default traces that are provided for this purpose. After the traces are cut, an external power supply can be used along with a current meter to measure the current used by the selected power rail. The power rail can then be reconnected to the system by placing a jumper across the cut trace.

4.5 Mictor Connector Definition

Connectors MC1 and MC2 can be used to connect a logic analyzer to the secondary PCI bus. See Table 4–3 for a listing of the signals for each logic analyzer POD.

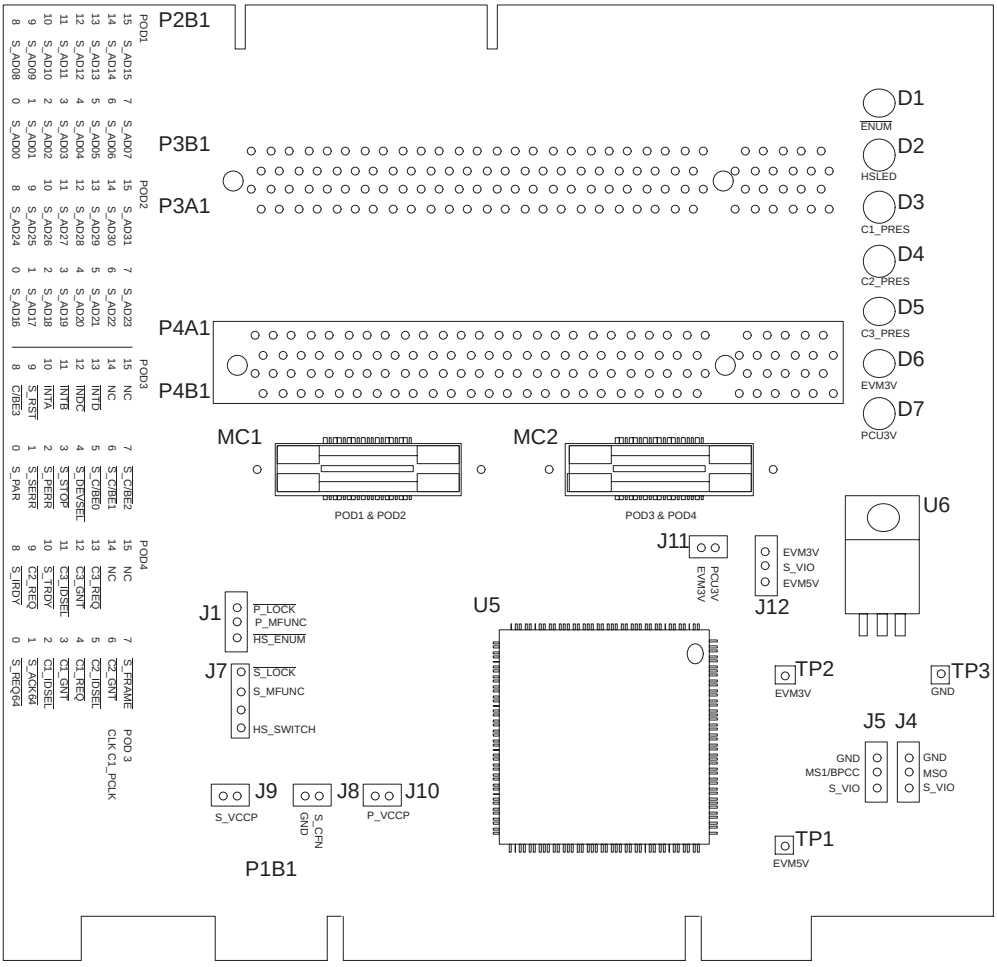
Table 4–3. HP Logic Analyzer POD Definition

Pin Number	POD 1	POD 2	POD 3	POD 4
0	S_AD0	S_AD16	S_PAR	$\overline{\text{S\_REQ64}}$
1	S_AD1	S_AD17	$\overline{\text{S\_SERR}}$	$\overline{\text{S\_ACK64}}$
2	S_AD2	S_AD18	$\overline{\text{S\_PERR}}$	C1_IDSEL
3	S_AD3	S_AD19	$\overline{\text{S\_STOP}}$	$\overline{\text{C1\_GNT}}$
4	S_AD4	S_AD20	$\overline{\text{S\_DEVSEL}}$	$\overline{\text{C1\_REQ}}$
5	S_AD5	S_AD21	$\overline{\text{S\_C/BE0}}$	C2_IDSEL
6	S_AD6	S_AD22	$\overline{\text{S\_C/BE1}}$	$\overline{\text{C2\_GNT}}$
7	S_AD7	S_AD23	$\overline{\text{S\_C/BE2}}$	$\overline{\text{S\_FRAME}}$
8	S_AD8	S_AD24	$\overline{\text{S\_C/BE3}}$	$\overline{\text{S\_IRDY}}$
9	S_AD9	S_AD25	$\overline{\text{S\_RST}}$	$\overline{\text{C2\_REQ}}$
10	S_AD10	S_AD26	$\overline{\text{INTA}}$	$\overline{\text{S\_TRDY}}$
11	S_AD11	S_AD27	$\overline{\text{INTB}}$	C3_IDSEL
12	S_AD12	S_AD28	$\overline{\text{INTC}}$	$\overline{\text{C3\_GNT}}$
13	S_AD13	S_AD29	$\overline{\text{INTD}}$	$\overline{\text{C3\_REQ}}$
14	S_AD14	S_AD30	NC	NC
15	S_AD15	S_AD31	NC	NC

4.6 Board Description

The board layout is shown in Figure 4–1. The schematic diagram of the board is in Figure 4–2. Table 4–4, bill of materials, is a list of the parts used to assemble the board.

Figure 4–1. Part and Jumper Locations



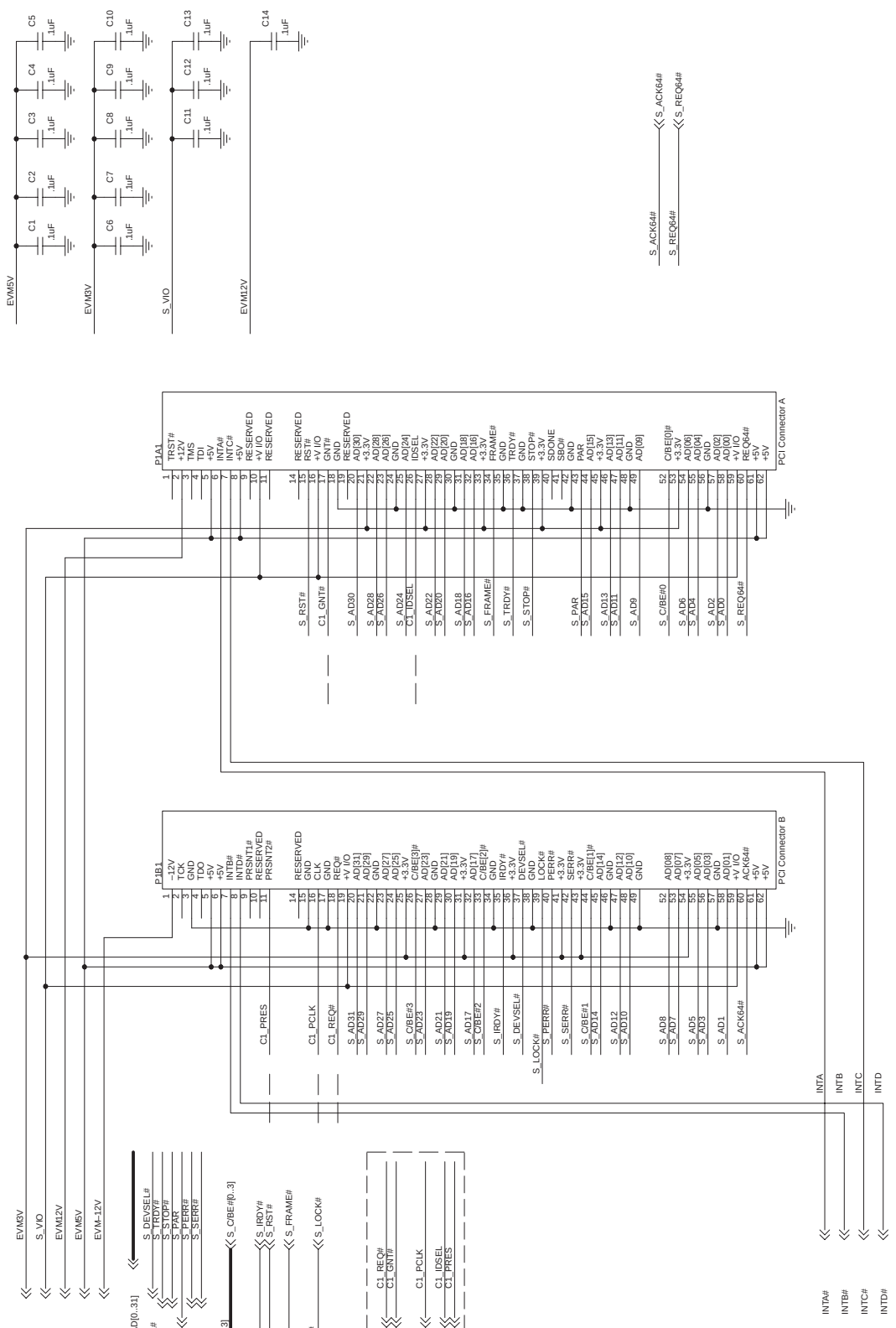


Figure 4–2. Schematic Diagram (Sheet 1 of 8)

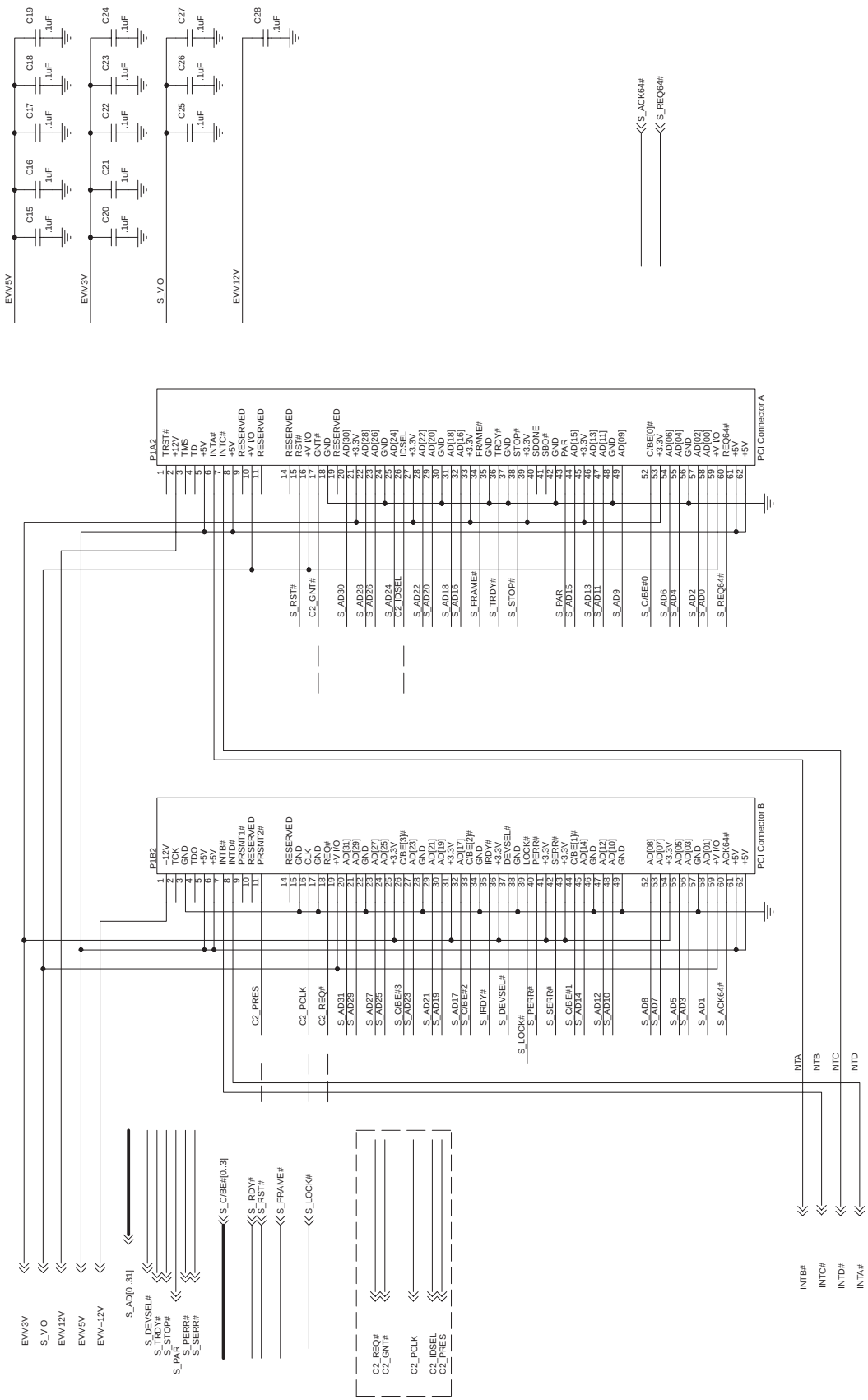


Figure 4–2. Schematic Diagram (Sheet 2 of 8)

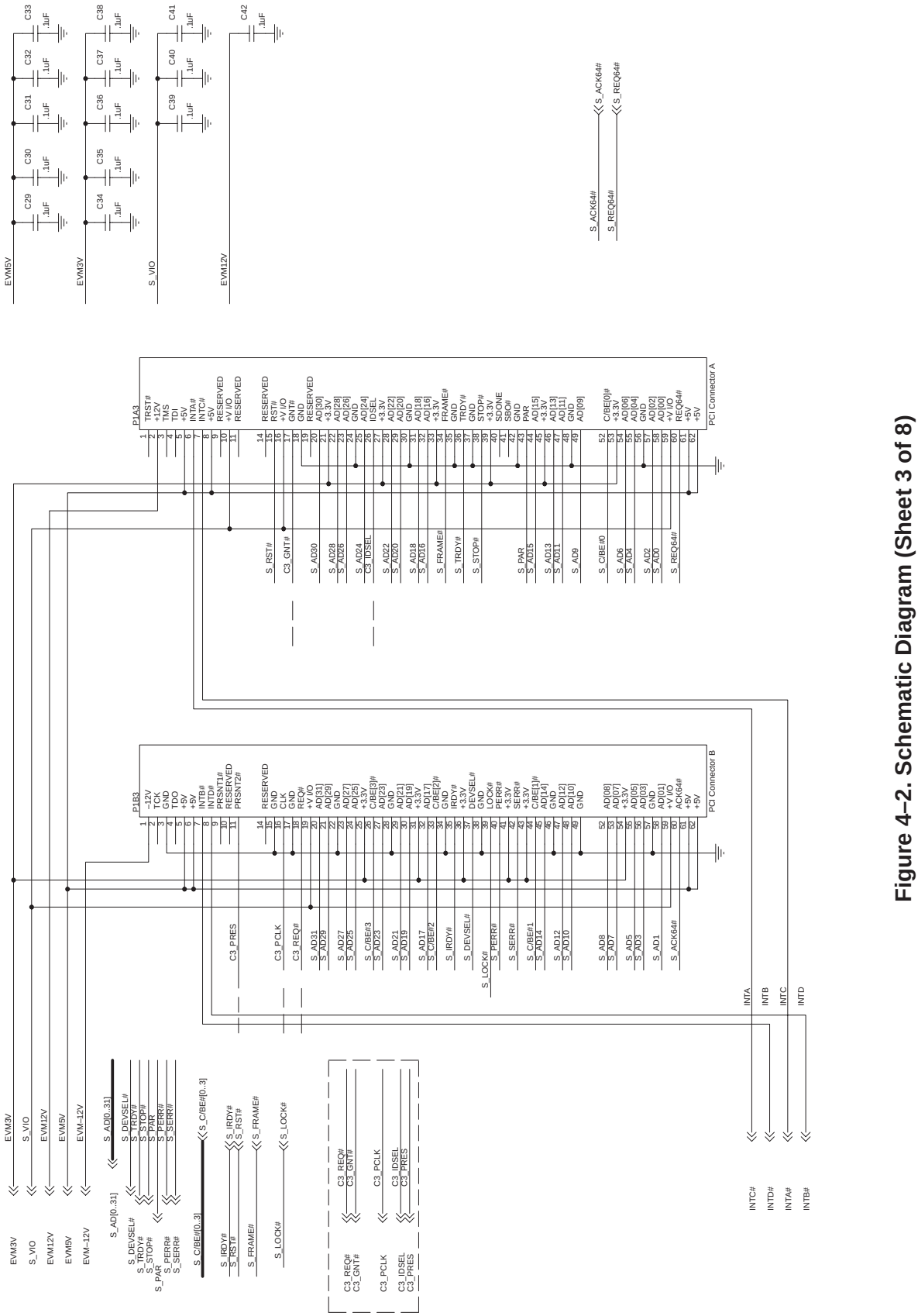


Figure 4–2. Schematic Diagram (Sheet 3 of 8)

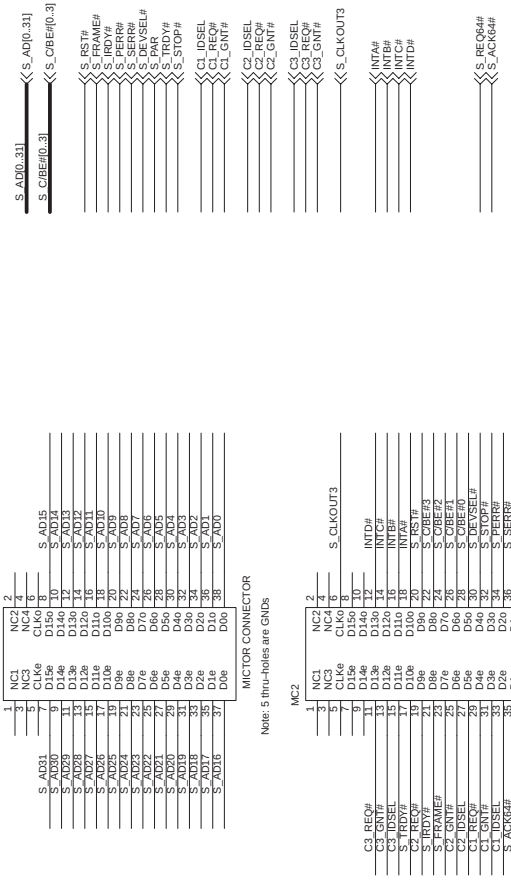


Figure 4–2. Schematic Diagram (Sheet 4 of 8)

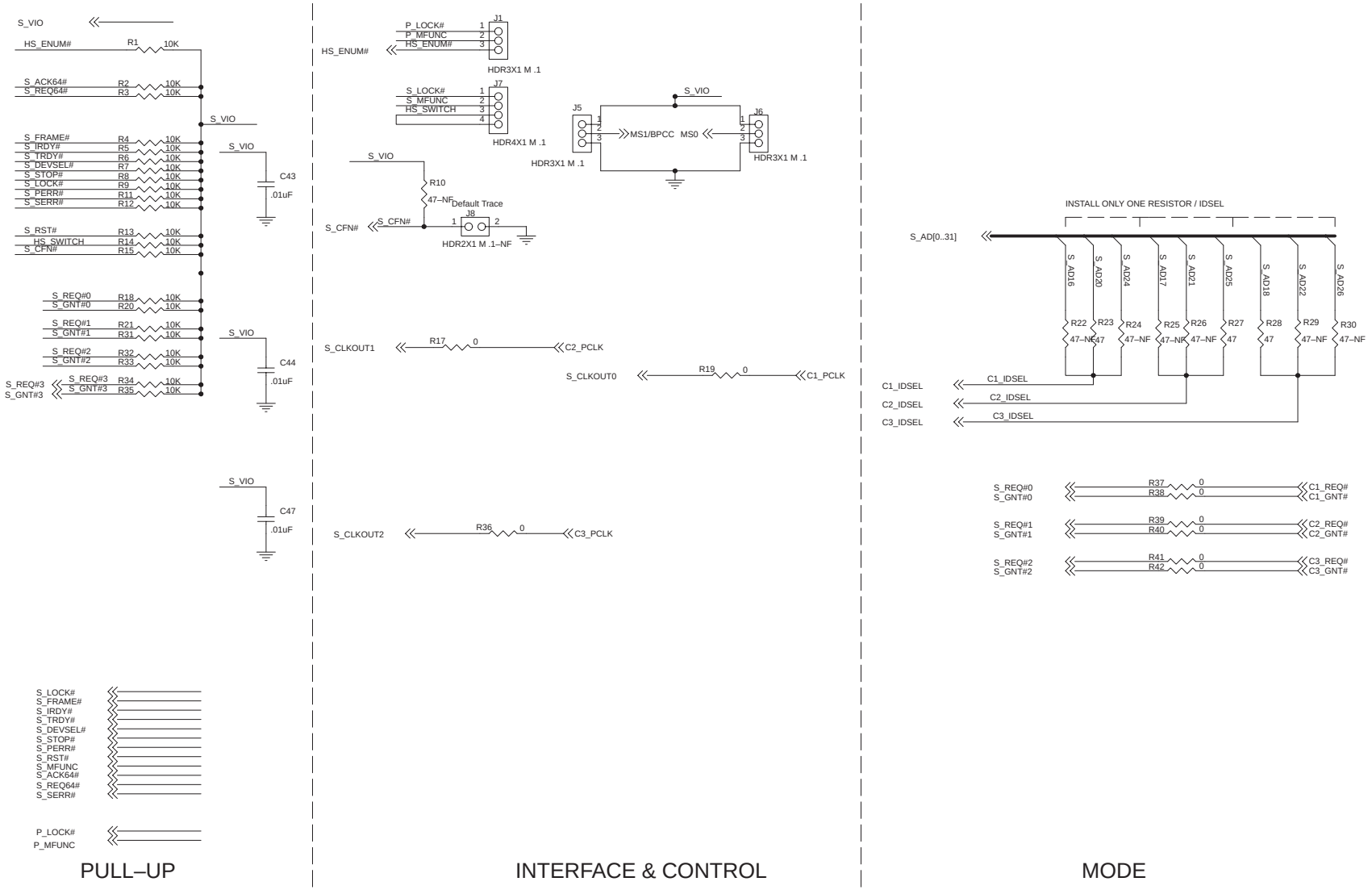


Figure 4–2. Schematic Diagram (Sheet 5 of 8)

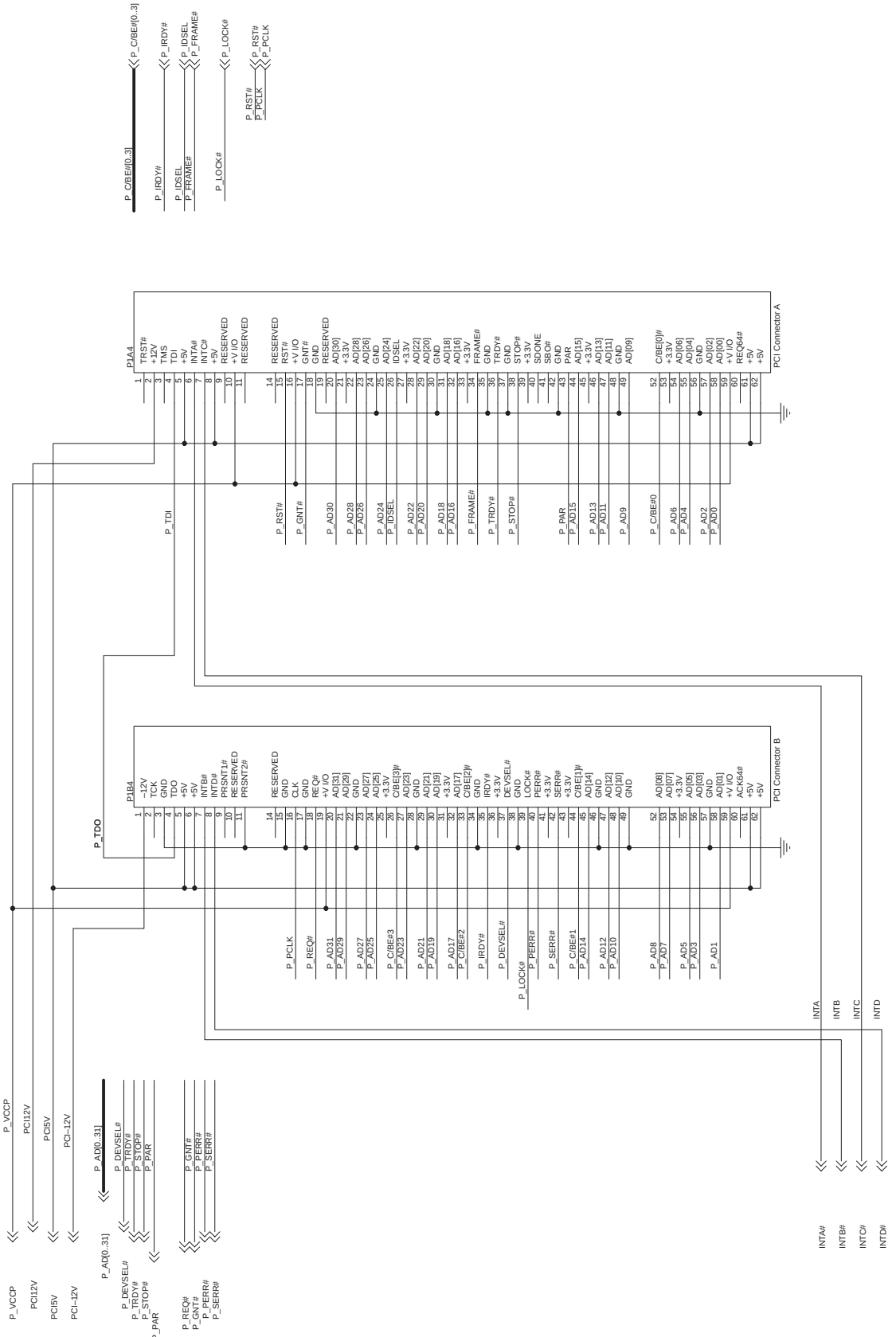


Figure 4–2. Schematic Diagram (Sheet 6 of 8)

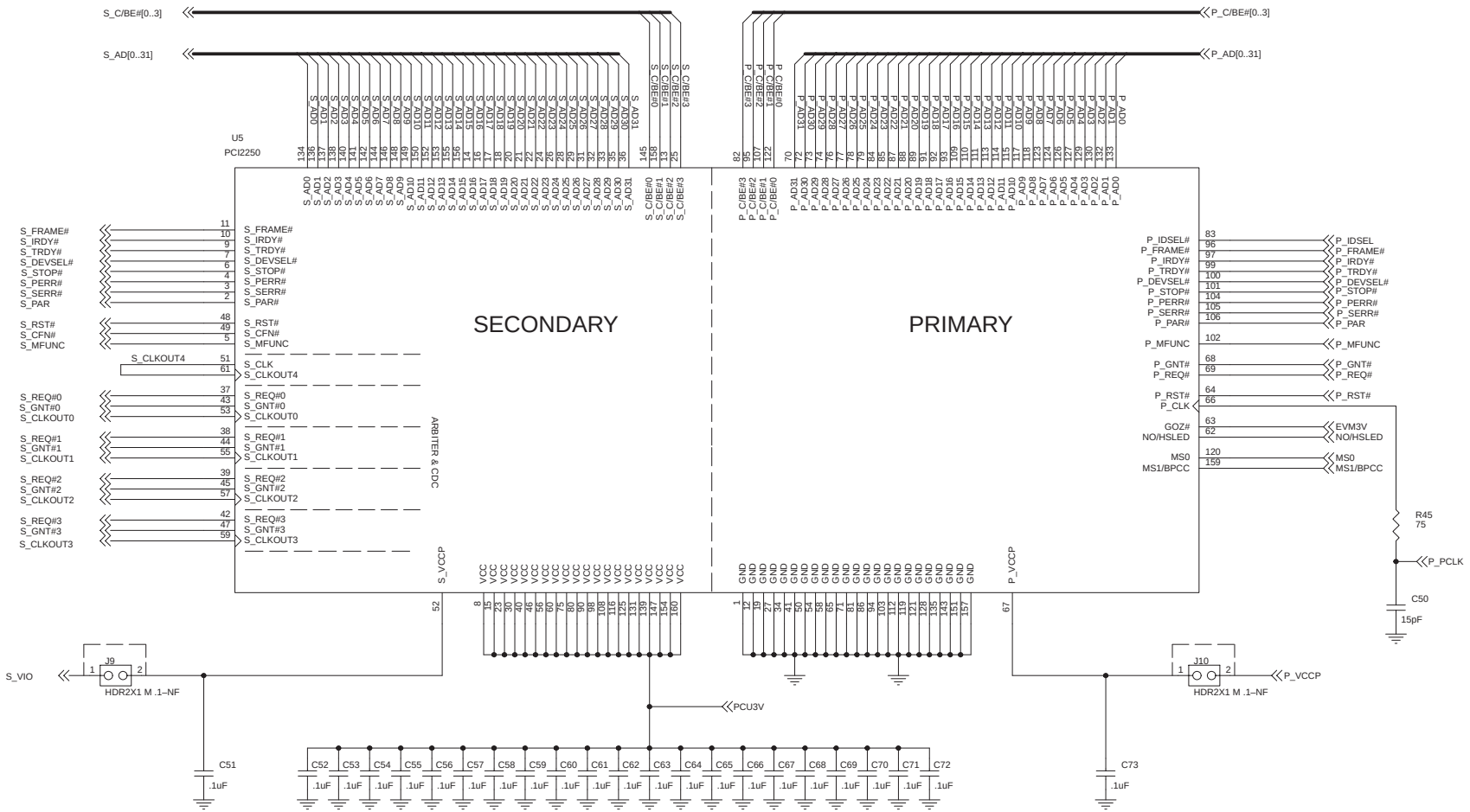


Figure 4–2. Schematic Diagram (Sheet 7 of 8)

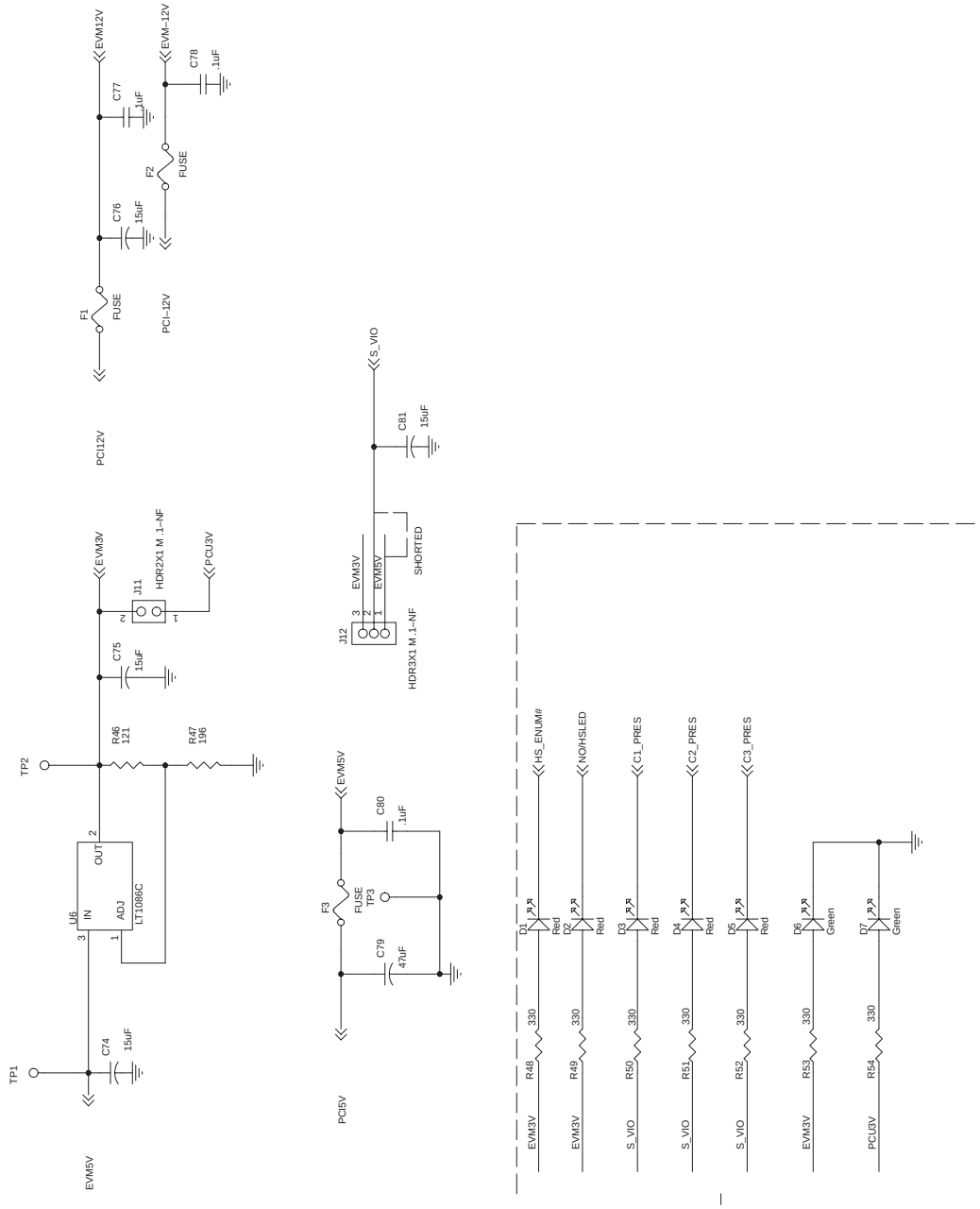


Figure 4–2. Schematic Diagram (Sheet 8 of 8)

Table 4–4. PCI2250 EVM Bill of Materials

Item	Qty	Reference	Part	Pkg	MFG	Part No.
1	68	C1–C42, C51–C73, C77, C78, C80	0.1 µF	805	Phillips	08052R104K9BB0
2	3	C43, C44, C47	0.01 µF	805	MMC	CE103K2NR
3	1	C50	15 pF	805	MMC	CE150J2NO
4	4	C74–C76, C81	15 µF	6032	NIC	NTC-T156K20TRC
5	1	C79	47 µF	6032	NIC	NTC-T476K6.3TRC
6	5	D1–D5	Red	See Diagram	Lumex	
7	2	D6, D7	Green	See Diagram	Lumex	
8	3	F1–F3	Fuse	TH	LittleFuse	251.75
9	3	J1, J5, J6	HDR3X1 M 0.1		AMP	103321-3
10	1	J7	HDR4X1 M 0.1		AMP	103321-4
11	4	J8–J11	HDR2X1 M 0.1-nF		AMP	103321-2
12	1	J12	HDR3X1 M 0.1-nF		AMP	103321-3
13	2	MC1, MC2	Mictor Connector		AMP	2-767004-2
14	2	P1A1/P1B1, P1A3/P1B3	PCI Connector	N/A	AMP	145154-8
15	1	P1A2/P1B2	PCI Connector		Capstone	CEE2X60SMV-3Z14W
16	22	R1–R9, R11–R15, R18, R20, R21, R31–R35	10K	805	KOA	RM73B2A103J
17	7	R10, R22, R24–R26, R29, R30	47 nF	805	KOA	RM73B2A470J
18	9	R17, R19, R36–R42	0	805	KOA	RM73Z2A000
19	3	R23, R27, R28	47	805	KOA	RM73B2A470J
20	1	R45	75	805	KOA	RM73B2A750J
21	1	R46	121	TH	NIC	NMR25F1210B
21	1	P1A2/P1B2	PCI Connector	N/A	Capstone	CEE2X60SMV-3Z14W
22	1	R47	196	TH	NIC	NMR25F1960B
23	7	R48–R54	330	805	KOA	RM73B2A331J
24	3	TP1–TP3	Test Point		AMP	
25	1	U5	PCI2250	See Drawing	Texas Instruments	PCI2250
26	1	U6	LT1086C	TO-220	Digi-Key	LT1086C